CLAIMS

What is Claimed is:

1. A method for detecting electrical defects on test structures of a semiconductor die, the test structures including a plurality of electrically-isolated test structures and a plurality of non-electrically-isolated test structures, the test structures each having a portion located partially within a scan area, the method comprising:

a. scanning the portion of the test structures located within the scan area to obtain voltage contrast images of the test structures' portions; and

b. in a multi-pixel processor, analyzing the obtained voltage contrast images to determine whether there are defects present within the test structures.

2. A method as recited in claim 1 wherein the multi-pixel processor operates with pixel resolution sizes in a range of about 25nm to 2000nm

3. A method as recited in claim 1, wherein the processor operates with a pixel size nominally equivalent to two times a width of the test structure's line width to maximize throughput at optimal signal to noise sensitivity.

4. A method as recited in claim 1 wherein the scanned portions of the electrically isolated test structures are expected to have substantially a same first brightness level, and the scanned portions of the non-electrically isolated test structures are expected to have substantially a same second brightness level that differs from the first brightness level.

5. A method as recited in claim 1 wherein the obtained voltage contrast images are analyzed by comparing them to a plurality of reference images.

6. A method as recited in claim 3 wherein the reference images are generated from a database.

7. A method as recited in claim 6 wherein the database comprises expected voltage contrast images.

8. A method as recited in claim 6 wherein the database is a design database utilized to fabricate the semiconductor die.

9. A method as recited in claim 1 wherein the obtained voltage contrast images are analyzed by comparing them to a truth table.

10. A method as recited in claim 9 wherein the truth table includes expected brightness levels for the scanned portions of the test structures.

11. A method as recited in claim 1 wherein the obtained voltage contrast images are analyzed by comparing them to a plurality of images from an adjacent semiconductor die.

12. A method as recited in claim 1 wherein the obtained voltage contrast images are analyzed by comparing them to a plurality of images from an adjacent other plurality of test structures on the semiconductor die.

13. A method as recited in claim 10 wherein the comparison is accomplished in an array mode.

14. A method as recited in claim 1 wherein the scanning is accomplished with an electron beam.

15. A computer-readable medium comprising computer code for detecting electrical defects on test structures of a semiconductor die, the test structures including a plurality of electrically-isolated test structures and a plurality of non-electrically-isolated test structures, the

test structures each having a portion located partially within a scan area, the computer-readable medium comprising:

computer code for obtaining voltage contrast images of the portions of the test structures located within the scan area; and

computer code for analyzing the obtained voltage contrast images to determine whether there are defects present within the test structures, the images being analyzed in a multi-pixel fashion.

16. A computer-readable medium as recited in claim 15 wherein the images of the portions of the electrically isolated test structures are expected to have substantially a same first brightness level, and the image of the portions of the non-electrically isolated test structures are expected to have substantially a same second brightness level that differs from the first brightness level.

17. A computer-readable medium as recited in claim 15 wherein the obtained voltage contrast images are analyzed by comparing them to a plurality of reference images.

18. A computer-readable medium as recited in claim 17 wherein the reference images are generated from a database.

19. A computer-readable medium as recited in claim 18 wherein the database comprises expected voltage contrast images.

20. A computer-readable medium as recited in claim 18 wherein the database is a design database utilized to fabricate the semiconductor die.

21. A computer-readable medium as recited in claim 15 wherein the obtained voltage contrast images are analyzed by comparing them to a truth table.

22. A computer-readable medium as recited in claim 21 wherein the truth table includes expected brightness levels for the scanned portions of the test structures.

23. A computer-readable medium as recited in claim 15 wherein the obtained voltage contrast images are analyzed by comparing them to a plurality of images from an adjacent semiconductor die.

24. A computer-readable medium as recited in claim 15 wherein the obtained voltage contrast images are analyzed by comparing them to a plurality of images from an adjacent other plurality of test structures on the semiconductor die.

25. A computer-readable medium as recited in claim 24 wherein the comparison is accomplished in an array mode.